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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,352	04/13/2004	Eun-ae Chung	5649-1299	4723

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EXAMINER	
KENNEDY, JENNIFER M	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,352	CHUNG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04, 3/05, 8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II, claims 17-30 in the reply filed on June 28, 2005 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27 recites the limitation "the doped poly$Si_{1-x}Ge_x$" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 17, from which claim 27 depends, does not refer to the silicon germanium layer as a doped poly layer. The examiner believes that claim 27 should depend from claim 18 for proper antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17, 26, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Thakur et al. (U.S. Patent No. 6,479,854).

Thakur et al. disclose a method of fabricating a capacitor of a semiconductor device the method comprising:

forming a capacitor lower electrode (30, 32) on a semiconductor substrate;

forming a dielectric layer (28) on the lower electrode and

sequentially stacking a metallic layer (26) and a $Si_{1-x}Ge_x$ layer (22) on the dielectric layer to form an upper electrode comprising the metallic layer and the $Si_{1-x}Ge_x$ layer (see Figure 2 and column 4, lines 25 through column 5, line 20).

In re claim 26, Thakur et al. disclose the method wherein the metallic layer of the upper electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof (see column 4, lines 25-35).

In re claim 28, Thakur et al. disclose the method wherein the lower electrode comprises a metallic layer (30, see column 4, lines 25-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 18-25, 27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thakur et al. (U.S. Patent No. 6,479,854) in view of Economikos et al. (U.S. Patent No. 6,180,480).

In re claim 18, Thakur et al. disclose the method as claimed and rejected above, but does not disclose the method wherein the silicon germanium layer is a doped poly$Si_{1-x}Ge_x$ layer, nor the method of doping.

Economikos et al. disclose the method of forming a doped poly $Si_{1-x}Ge_x$ layer (see column 3, line 40 through column 4, line 25) and the method of doping the poly $Si_{1-x}Ge_x$ layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a doped poly layer by the method of Economikos in the method of Thakur et al. because as Economikos et al. disclose the layer must be doped in order to create an electrically conductive layer (see column 4, lines 20-25).

In re claim 19, the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is formed by doping a poly $Si_{1-x}Ge_x$ layer with P or As (see Economikos et al. column 4, lines 15-25).

In re claim 20, the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is formed by doping a poly $Si_{1-x}Ge_x$ layer with B (see Economikos et al. column 4, lines 15-25).

In re claim 21, the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is formed by depositing a poly$Si_{1-x}Ge_x$ while simultaneously doping impurities (an in situ process, see Economikos et al. column 4, lines 15-25).

In re claim 22 and 23, the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is deposited and simultaneously activated at temperatures between about 350°C and 550°C (see temperatures of Economikos et al. at column 3, line 40 through column 4, line 4, some of which are sufficient to activate).

In re claim 24 and 25, the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is deposited and then activation and thermal treatment is performed at a temperature between about 400°C and 550°C (see Economikos et al. column 4, lines 45-50).

In re claim 27 the combined Thakur et al. and Economikos et al. disclose the method wherein the doped poly $Si_{1-x}Ge_x$ layer is formed using LPCVD using furnace

type equipment, single wafer type equipment and/ or mini-batch equipment (see Economikos et al. column 3, lines 40-53).

In re claim 29, Thakur et al. disclose a method of fabricating a capacitor of a semiconductor device the method comprising:

forming a capacitor lower electrode (30, 32) on a semiconductor substrate;

forming a dielectric layer (28) on the lower electrode and

forming a a $Si_{1-x}Ge_x$ layer (22) on the dielectric layer (see Figure 2 and column 4, lines 25 through column 5, line 20).

Thakur et al. does not disclose the conditions under which the $Si_{1-x}Ge_x$ layer is formed. Economikos et al. disclose the method wherein the $Si_{1-x}Ge_x$ layer is formed at about 550°C or less (see column 3, line 40 through column 4, line 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the $Si_{1-x}Ge_x$ layer of Thakur et al. at a temperature of 550°C or less, because as Economikos et al. discloses the temperature provides for a highly conformal deposition allowing for deposition in high aspect ratio openings such as seen in Thakur et al.

In re claim 30, the combined Thakur et al. and Economikos et al. disclose the method further comprising thermally treating the $Si_{1-x}Ge_x$ layer at about 550°C or less (see Economikos et al. column 4, lines 45-50).

Claims 17, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine et al. (U.S. Patent No. 6,511,873) in view of Thakur et al. (U.S. Patent No. 6,479,854).

Ballentine et al. disclose a method of fabricating a capacitor of a semiconductor device the method comprising:

forming a capacitor lower electrode (12, 20) on a semiconductor substrate;

forming a dielectric layer (14) on the lower electrode and

sequentially stacking a diffusion barrier layer (20) and a $Si_{1-x}Ge_x$ layer (16) on the dielectric layer to form an upper electrode comprising the metallic layer and the $Si_{1-x}Ge_x$ layer.

Ballentine et al. disclose the method of forming the diffusion barrier layer of nitrides, oxides and oxynitride but does note disclose that the layer is a metallic oxide or nitride. Thakur et al. discloses the method of utilizing metallic oxides and nitrides for use as barrier layers (see column 4, lines 25-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the diffusion barrier layers of Ballentine with the materials of Thakur et al., because, as Thakur et al. teach these materials are convention barrier materials that prevent leakage of the capacitor (see column 4, lines 25-45) and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

In re claim 26, the combined Ballentine et al. and Thakur et al. disclose the method wherein the metallic layer of the upper electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof (see Thakur et al., column 4, lines 25-35).

In re claim 28, the combined Ballentine et al. and Thakur et al. discloses the method wherein the lower electrode comprises a metallic layer (see Thakur et al. 30, see column 4, lines 25-35).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rhee et al. discloses the crystallizaion temperature of silicon germanium.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy

JENNIFER KENNEDY
PRIMARY EXAMINER